Abstract—An original active resistor structure using exclusively MOS devices working in the saturation region will be further presented. Performing the great advantage of an excellent linearity, obtained by a proper biasing of the differential core (using original translation and arithmetical mean blocks), the proposed circuit is designed for low-voltage low-power operation and allows a very good controllability of the equivalent resistance. The estimated linearity is obtained for an extended range of the differential input voltage and in the worst case of considering second-order effects that affect MOS transistors operation. The frequency response of the new active resistor is strongly increased by operating all MOS devices in the saturation region. The circuit is implemented in 0.35μm CMOS technology on a die area of 30μm × 40μm, being supplied at ±3.6V. The active resistor presents a very good linearity (THD < 0.8%) for an extended range of the input voltage (−2.5V < VIN < 2.5V). The tuning range is extremely large comparing with the previous reported active resistors: ±(500Ω < 5Ω)Ω, the circuit being able to simulate both positive and negative active resistances.

Index Terms—Linearity, equivalent active resistance, differential amplifier, second-order effects

I. INTRODUCTION

CMOS active resistors are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilisation domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic.

An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, finding very large domains of applications such as the canceling of an operational amplifier load or the design of Deboo integrators with improved performances.

The first generation of MOS active resistors [1], [2] used MOS transistors working in the linear region. The main disadvantage is that the realised active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters.

A better design of MOS active resistors is based on MOS transistors working in saturation [3]-[15]. Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. Usually, the resulting linearisation of the I−V characteristic is obtained by a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and channel-length modulation effect) limits the circuit linearity introducing odd and even-order distortions, as shown in [4]. For this reason, an improved linearisation technique has to be design in order to compensate the nonlinearities introduced by the second-order effects.

II. THEORETICAL ANALYSIS

The original proposed active resistor circuit is based on a quasi-symmetrical differential structure, using exclusively MOS devices operating in the saturation region for improving the circuit frequency response. In order to improve the active resistor linearity, a proper biasing of the differential core will be used, based on original translation and arithmetical mean blocks. As a result of applying original design techniques, the circuit linearity is maintained for an extended range of the differential input voltage, even in the case of considering second-order effects that affect MOS transistors operation

A. The block diagram of the active resistor circuit

The block diagram of the proposed active resistor is presented in Figure 1. The “DA” block represents a classical active-load differential amplifier, having the common-sources point biased at a potential V fixed by the circuit “M”. This circuit computes the arithmetical mean of input potentials, assuring a very good linearity of the entire structure, with the contribution of “T” blocks (which are used for introducing a translation of input potentials). Output currents of the “DA” block are forces to pass through the input pins, assuring, in this way, a linear current-voltage characteristic $i_Q(v_{1'} - v_{1})$ of the active resistor structure, so a constant equivalent resistance.

B. The “DA” (Differential Amplifier) block

The “DA” block is implemented as a classical active-load differential amplifier, having the concrete realization presented in Figure 2.

Considering a saturation operation of the MOS devices from Figure 2, the output current of the differential amplifier could be expressed as:

$$i_O = i_{DIA} + i_{DIB} = \frac{K}{2}(v_{SGIA} - V_T)^2 - \frac{K}{2}(v_{SGIB} - V_T)^2, \quad (1)$$

equivalent with:

$$i_O = \frac{K}{2}(v_{SGIA} - v_{SGIB}) \cdot v_{SGIA} + v_{SGIB} - 2V_T. \quad (2)$$

Because:

$$v_{SGIA} = V - v_{1C} \quad (3)$$
and:
\[ v_{SG1d'} = V - v_{IC'}, \]  
(4)

it results:
\[ i_O = \frac{K}{2} \left( v_{IC} - v_{IC'} \right) \left( 2V - v_{IC} - v_{IC'} - 2V_T \right). \]  
(5)

In order to obtain a linear transfer characteristic \( i_O(v_{IC} - v_{IC'}) \), it is necessary that the second parenthesis from (5) to be constant with respect to the differential input voltage \( v_{IC} - v_{IC'} \):
\[ 2V - v_{IC} - v_{IC'} - 2V_T = A = c.t., \]  
(6)

resulting the necessity of implementing a voltage \( V \) equal with:
\[ V = \frac{v_{IC} + v_{IC'}}{2} + V_T + \frac{A}{2}. \]  
(7)

C. The “T” (Translation) block

The translation of the \( V \) potential by \( V_T + A/2 \) (relation (7)) could be obtained by the “T” block, having the implementation proposed in Figure 3.

Because the same current \( i_O \) is passing through all transistors from Figure 3, it is possible to write that:
\[ i_O = \frac{4K}{2} \left( \frac{v_I - v_{IC}}{2} - V_T \right)^2 = \frac{K}{2} \left( V_C - V_T \right)^2, \]  
(8)

resulting:
\[ v_I = v_{IC} + V_C + V_T \]  
(9)

and:
\[ v_I' = v_{IC'} + V_C + V_T. \]  
(10)

So, both input potentials \( v_I \) and \( v_I' \) are shifted with the same amount, \( V_T + V_C \).

D. The “M” (arithmetical Mean) block

In order to obtain the arithmetical mean of input potentials expressed by relation (8), the circuit from Figure 4 will be proposed, having the advantage of using only MOS transistors biased in saturation region.

The differential amplifiers \( T_{14} - T_{15} \) and \( T_{14'} - T_{15'} \) are biased at the same current, \( i_O \) and, additionally, the sum of drain currents of \( T_{15} \) and \( T_{15'} \) transistors are, also, equal with \( i_O \). As a result, gate-source voltages of \( T_{14} \) and \( T_{14'} \) transistors are equal and, similarly, gate-source voltages of \( T_{15} \) and \( T_{15'} \) transistors are equal. In order to obtain the expression of voltage \( V \), is is possible to write that:
\[ v_I - V = v_{GS14} - v_{GS15} \]  
(11)

and:
\[ V - v_I' = v_{GS14'} - v_{GS15'}. \]  
(12)

Subtracting these two relations and using the previous observations, it results that:
\[ v_I = v_I + v_{I'} \]  
(13)

Replacing (9) and (10) in (13), it could be obtained:
\[ V = \frac{v_I + v_{I'}}{2}. \]  
(14)

Comparing relations (7) and (14), it results that \( A = 2V_C \), so:
\[ i_O = K \left( v_{I} - v_{I'} \right), \]  
(15)
equivalent (using (9) and (10)) with:
\[ i_O = K \left( v_{I} - v_{I'} \right) = G_m \left( v_{I} - v_{I'} \right), \]  
(16)

\( G_m = K \) being the equivalent transconductance of the differential amplifier. In conclusion, a linear transfer characteristic of the differential structure having the block diagram presented in Figure 1 has been obtained by using an original biasing of the classical differential amplifier from Figure 2. The full implementation of the linearized differential structure is presented in Figure 5.

E. The active resistor circuit

Because output currents of the “DA” block are forces to pass through the input pins (Figure 1), a linear current-voltage characteristic \( i_O(v_I - v_I') \) of the active resistor structure will be obtained. So, a constant equivalent resistance of the entire structure from Figure 1 could be achieved:
As a result of using translation blocks from Figure 3, the transconductance \( G_m \) of the differential core will be not dependent on the threshold voltage, so the active resistor linearity will be not affected by the bulk effect.

\[ R_{ech} = \frac{v_1 - v_1'}{i_O} = \frac{I}{G_m} = \frac{I}{KV_C}. \]  \hspace{1cm} (17)

Figure 5. The full implementation of the differential structure

F. Second-order effects

The perfect linearity of the proposed active resistor structure expressed by (17) could be obtained only in a first-order analysis. All circuits presented above are affected by the second-order effects that degrade the quadratic law of the MOS transistor. These undesired effects are modeled by the following relations (channel-length modulation and mobility degradation).

\[ i_D = \frac{K}{2} (V_{GS} - V_T) \left( 1 + \lambda V_{SD} \right) \]  \hspace{1cm} (18)

\[ K = \frac{K \theta}{[1 + \theta G (V_{SG} - V_T)] [1 + \theta G (V_{SG} - V_T)]} \]  \hspace{1cm} (19)

Considering that the design condition \( \lambda = \theta G \) is fulfilled, drain currents of transistors \( T_1 \) and \( T_1' \) from Figure 2 will have the following expressions:

\[ i_{D1} = \frac{K}{2} x^2 \]  \hspace{1cm} (20)

and:

\[ i_{D1}' = \frac{K}{2} x'^2 \]  \hspace{1cm} (21)

where \( x = V_{SG1} - V_T \) and \( x' = V_{SG1} - V_T \). In this case, the consideration of second-order effects will conduct to the following expression of the output current of the differential amplifier “DA”:

\[ i_O = \frac{K}{2} \left( \frac{x^2}{1 + \theta G x} - \frac{x'^2}{1 + \theta G x'} \right). \]  \hspace{1cm} (22)

Because \( \theta G x << 1 \) and \( \theta G x' << 1 \), after some computations it is possible to write that:

\[ i_O = K V_C (v_1 - v_1') + \varepsilon, \]  \hspace{1cm} (23)

\( \varepsilon \) being the error caused by second-order effects:

\[ \varepsilon = \frac{3 K G}{2} \left( v_1 - v_1' \right)^2 + \frac{K G}{8} \left( v_1 - v_1' \right)^3. \]  \hspace{1cm} (24)

Because the first term of (24) is linearly dependent of the differential input voltage of the differential amplifier “DA”, \( v_1 - v_1' \), its presence will be concretize in a very small changing of the main term from (23), \( K V_C (v_1 - v_1') \). Thus, the total harmonic distortion coefficient of the circuit could be expressed as the ratio of the second term from (24) – third-order term – and the linear term from (23), resulting:

\[ THD_3 = \frac{\theta G}{8 V_C} (v_1 - v_1')^2. \]  \hspace{1cm} (25)

The circuit distortions are strongly increased when the amplitude of the differential voltage applied at the input of the circuit increases. It is possible to reduce the value of the total harmonic distortion coefficient even for large values of the input voltage amplitude by using an anti-parallel connection of two differential amplifiers properly designed and having different biasing.

III. SIMULATED RESULTS

The circuit was implemented in 0.35\( \mu \)m CMOS technology on a die area of 30\( \mu \)m \( \times \) 40\( \mu \)m, being supplied at \( \pm 3.6 V \). The SPICE simulation of the proposed active resistor structure is presented in Figure 6. The circuit presents a very good linearity (THD < 0.8\% ) for an extended range of the input voltage \( (-2.5V < V_x - V_y < 2.5V) \). The tuning range is extremely large comparing with the previous reported active resistors: \( \pm (500k\Omega - 5M\Omega) \), the circuit
being able to simulate both positive and negative active resistances. An other important advantage of the proposed structure is referring to the possibility of operating also as floating resistor and as ground-connected resistor.

V. CONCLUSIONS

An original active resistor structure using exclusively MOS devices working in the saturation region has been presented. Performing the great advantage of an excellent linearity, obtained by a proper biasing of the differential core (using original translation and arithmetical mean blocks), the proposed circuit is designed for low-voltage low-power operation and allows a very good controllability of the equivalent resistance. The estimated linearity is obtained for an extended range of the differential input voltage and in the worst case of considering second-order effects that affect MOS transistors operation. The frequency response of the new active resistor is strongly increased by operating all MOS transistors in the saturation region.

A comparison between the proposed circuit and the previous reported active resistors is presented in Table 1.

<table>
<thead>
<tr>
<th>Techn. (µm)</th>
<th>Supply voltage (V)</th>
<th>Operatin g range (V)</th>
<th>Tuning range</th>
<th>THD (%)</th>
<th>Floating</th>
<th>Negative resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>±3.6</td>
<td>±2.5</td>
<td>±(500kΩ-5MΩ)</td>
<td>0.8</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>[6]</td>
<td>2</td>
<td>10</td>
<td>2.4</td>
<td>56-112kΩ</td>
<td>1</td>
<td>yes</td>
</tr>
<tr>
<td>[7]</td>
<td>3</td>
<td>10</td>
<td>8</td>
<td>-</td>
<td>±1</td>
<td>no</td>
</tr>
<tr>
<td>[8]</td>
<td>2</td>
<td>5</td>
<td>3</td>
<td>±5%</td>
<td>0.01</td>
<td>no</td>
</tr>
<tr>
<td>[9] BiCMOS</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>0.0032</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>[10]</td>
<td>0.5</td>
<td>3</td>
<td>2</td>
<td>-</td>
<td>1</td>
<td>no</td>
</tr>
<tr>
<td>[11]</td>
<td>0.5</td>
<td>3.6</td>
<td>2.5</td>
<td>-</td>
<td>0.2</td>
<td>no</td>
</tr>
<tr>
<td>[12]</td>
<td>0.8</td>
<td>3</td>
<td>3</td>
<td>&lt; 93.3kΩ</td>
<td>-</td>
<td>yes</td>
</tr>
<tr>
<td>[13]</td>
<td>1.5</td>
<td>±5V</td>
<td>-</td>
<td>2.6-5.1MΩ</td>
<td>-</td>
<td>yes</td>
</tr>
</tbody>
</table>

REFERENCES


