Channel Coding and Carrier Recovery for Adaptive Modulation Microwave Radio Links

Stefano Chinnici\textsuperscript{1}, Carmelo Decanis\textsuperscript{2}

\textsuperscript{1}Ericsson Telecomunicazioni S.p.A
Milano - Italy.
\textsuperscript{2}stefano.chinnici@ericsson.com
carmelo.decanis@ericsson.com

Abstract—This paper deals with channel coding and carrier recovery design for high-speed adaptive modulation microwave radio transmission systems. The challenges posed by the microwave channel are discussed and the design trade-offs are analyzed. The proposed flexible adaptive modulation solution employs M-QAM modulations from 4 QAM up to 512 QAM and a high rate LDPC code. The code-rate flexible LDPC code performs within 1 dB away from the pragmatic capacity in AWGN channel. Particular attention is paid to the design of the carrier synchronization algorithm working at the low SNR conditions imposed by the code and the relatively poor local oscillator behavior.

I. INTRODUCTION

Broadband fixed radio links are a reasonably cheap technological solution to communicate high data rate information between base transceiver stations and base station controller and/or between the latter and the mobile service switching center, with data rates spanning from tenths of Mb/s to close to 1 Gb/s depending on the positioning in the mobile backhaul network. To cope with different user needs, and to satisfy the ever increasing request for large throughputs and high quality of service, the modems must jointly satisfy the requirements of versatility, bandwidth/power efficiency, and very low bit/frame error probabilities. To be jointly met, these requirements impose the use of modulator alphabets with large cardinality, to be used in a pragmatic, or bit-interleaved [5] way with variable-rate powerful codes yielding performance close to the information-theoretical limits with low error floors and a manageable hardware complexity. In terms of modulation, 64, 128, 256 and 512-QAM are the main candidates in fixed radio-links but low-order constellations, down to 4 QAM, are required for adaptive links. When it comes to channel coding the largely deployed scheme based on concatenation of outer Reed-Solomon and inner binary codes needs to be replaced by new schemes based on turbo-like [6][7] or low-density parity-check (LDPC) codes. The extremely good performance of these classes of codes makes the receiver front-end work at extremely low values of the signal-to-noise ratio, thus leading to a challenging design of the synchronization algorithms, with particular emphasis on the carrier recovery functionality that must also cope with a high level of phase noise imposed by the overall low cost constraint.

Also, to reach very high data rates, like 1 Gbit/s, and to match rather stringent latency requirements, the channel coding design must be compatible with a decoder structure possessing a high degree of parallelism. Turbo-like and LDPC codes offer a high degree of parallelism without memory-access collisions [8] by a proper design of the interleaver (for turbo-like codes) and of the parity-check matrix (for the LDPC codes). Both classes of codes can be made flexible to support a wide range of rates and block sizes. This explains the almost general tendency of recent transmission standards to replace the previous coding scheme with either turbo or LDPC codes (DVB, UMTS, 802).

This paper presents the design of a flexible coded modulation solution for fixed radio channels systems based on the use of a variable rate LDPC code and a suitable carrier recovery algorithm. Within the vast family of LDPC codes, we have chosen the class of quasi-cyclic, regular LDPC (QC-LDPC) codes [9] as candidate codes. These codes are structured codes based on algebraic and combinatorial constructions, endowed with a linear encoding complexity and very low decoding complexity. In spite of being regular LDPC codes, a property that leads in general to poorer performance than irregular, when properly designed they have been shown to yield performance almost as good as the irregular ones. Regularity also has simplifying consequences on the decoder design and structure.

Latency constraints in the application at hand set an upper limit to the codes block length, in the order of 10,000 bits, while the required high throughput places the lower limit to the code rate around 0.9.

The structure of the paper is the following. In section II we consider the microwave radio channel limitations in conjunction with the specific requirements of adaptive modulation, in section III the choices made in designing the code are discussed and section IV briefly outlines our search for a carrier recovery solution which can cope with the relatively poor phase stability of the local oscillators used in our application. Section V reports the performance of the proposed solution, obtained through simulation, along with the comparison with theoretical capacity limits. The
performance evaluation has been made assuming an AWGN channel with/without the contribution of the local oscillator phase noise. In the conclusive section we summarize the results and look forward to further developments, which include the implementation of the proposed FEC scheme in an FPGA-based adaptive modulation modem prototype.

II. THE MICROWAVE RADIO CHANNEL

A. General Considerations

The point-to-point wideband radio channel poses a number of requirements on the selection of the code-modulation pair selection. Under normal operating conditions, assuming that the receiver includes a digital channel equalizer, the channel can be modeled as an AWGN channel affected by a relative large phase noise, due to the medium-low characteristics of the local oscillator.

Network topology in the mobile backhaul cellular network usually requires cascading several point-to-point radio links with increasing link capacity. Latency requirements therefore make the retransmission of packets through ARQ strategies unfeasible. This in turn results in tight requirements on the residual bit error probability (BEP) of the whole link, which has to be below $10^{-11}$. Another resulting requirement is the single link must have a relatively low latency, of the order of a few milliseconds.

On the other hand, as large as possible coding gains are required, as they directly translate in a corresponding system gain, provided that the receiver front-end can cope with the resulting low value of the signal-to-noise ratio (SNR). Together, the two requirements ask for codes with both low convergence threshold and error floor.

To be able to adjust the net traffic capacity in different network segments with respect to FEC overhead and error-correction capability, the FEC must support different code rates.

A good code for microwave radio channels should therefore have moderate block lengths and a large coding gain maintained in all portions of the BEP curve. i.e. with a BEP curve slope not degraded at medium-high SNR levels. In addition, it must be possible with a limited hardware overhead to implement codes with different rates.

B. Phase Noise Effects

As already mentioned, total phase noise due to microwave oscillators results in additional degradation over the ideal AWGN channel model. Owing to the relatively low bandwidth of the underlying random process, the phase noise introduces correlation in the error events affecting the received code words. This phenomenon must be effectively counteracted through a proper design of the carrier recovery circuit, and with the possible addition of interleaving to break error correlation before the FEC decoder.

<table>
<thead>
<tr>
<th>Rate</th>
<th>Size</th>
<th>Circulants</th>
<th>Span</th>
</tr>
</thead>
<tbody>
<tr>
<td>15/16</td>
<td>511 x 8176</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>13/14</td>
<td>511 x 7154</td>
<td>14</td>
<td>56</td>
</tr>
<tr>
<td>11/12</td>
<td>511 x 6132</td>
<td>12</td>
<td>48</td>
</tr>
<tr>
<td>9/10</td>
<td>511 x 5110</td>
<td>10</td>
<td>40</td>
</tr>
</tbody>
</table>

*Note that the surviving circulants are always the leftmost ones.*

Given a certain spectral purity for microwave oscillators, the effect of phase noise is worse in narrower radio channels. Considering that in the typical network topology the traffic capacity increases in the levels farthest from the access points, the same code should have good performance in ideal AWGN as well as reasonable burst error correction capabilities.

III. Code Design

A. Targets

In the previous section we saw that low HW complexity, good coding gain at low SNR levels, absence of error floor at medium-high SNR levels, reasonable burst error robustness, moderate block lengths and code rate flexibility are required for the application under consideration. The code design was based on the following constraints/targets:

- code rates in the range (9/10, 15/16)
- block length not exceeding 9 kilobits
- at least 1.5 extra coding gain on the AWGN channel with respect to a Reed-Solomon based concatenated coding scheme with the same rate.

B. Regular vs. Irregular LDPC Codes

When considering the trade-off between regular and irregular code, both performance and hardware complexity must be taken into account. While it is known [10] that irregular codes yield an advantage in terms of performance in the convergence abscissa (waterfall region), and can be designed to show good error floor behavior [11], a regular construction lends itself to a simpler co-decoder implementation. For this reason, the choice went in favor of a regular LDPC code.

C. Random vs. Structured Codes

Irregular, random LDPC codes as designed in [10] based on certain guidelines and required structural properties have shown performance as close as desired to the capacity limits provided that there is no upper limit to the block length. Structured codes, on the other hand, can offer a lower hardware complexity of the encoder-decoder pair, owing to their algebraic or regular combinatorial structure.

D. Code Structure

The class of QC-LDPC codes [9,12] offers, for the block lengths of interests, good performance close to the best irregular, random codes, both in terms of convergence abscissa and error floor. In addition these codes have the advantage admitting a low-complexity encoder, and they can be effectively designed to include good burst error correction properties.
The proposed code is based on a quasi-cyclic structure, where the parity-check matrix is composed of square submatrices with cyclic structure (circulants). The highest code rate of 15/16 is reached with a parity-check matrix that concatenates 16 square circulants with 511 rows and columns, with row weight equal to column weight equal to 4. The resulting parity-check matrix has 32,704 non-zero entries, (constant) row weight equal to 64, (constant) column weight equal to 4, and describes a (8,176, 7,665) regular QC-LDPC code.

The circulants construction has been optimized using a computer search program that tries to find the solution best matching the following criteria:
- the zero-covering span of the code, a parameter that yields a lower bound on the erasure-burst-correction capability [13] should be maximized
- the row-column (RC) constraint, imposing that no two rows (or columns) have more than one 1-component in common, must be met, avoiding the short cycles of length 4 that heavily affect the code performance.

Since for parity-check matrices with quasi cyclic structure obeying the R-C constraint the minimum distance is at least equal to the column weight +1 (see [12]), the lower bound on minimum distance is 5.

The optimized code has a zero-covering span equal to 248. Over the binary erasure channel, the lower bound to the erasure-burst-correction capability of the code is 249 erasures ([13]). Using a large value for the zero-covering span as a design criterion is equivalent to assume that a good erasure-burst-correction capability of the code leads also to a good burst correction capability over the AWGN channel affected by correlated phase noise. The validity of this qualitative assumption has been checked by simulation.

E. Code Rate Flexibility

The code rate flexibility has been obtained by applying shortening to the “mother” 15/16 above described code. Shortened parity matrices are obtained from the 15/16 code parity-check matrix by removing a suitable number of rightmost circulants. The main codes parameters based on this construction are reported in Table I. When obtained by shortening a mother code matrix with the highest rate, the code rate flexibility induces a reduction of the block length, in turn leading to a larger gap from the infinite-length capacity limit at lower code rates. For all shortened codes the obtained zero-covering span is equal to 239, slightly lower than the value found for the mother code.

F. Expected Performance

In order to get some analytical indications on the expected performance, an attempt to estimate the minimum distance of the codes has been tried, beyond the zero-covering span. In fact, although other code properties can be related to the error floor [14], the minimum distance of the code sets a lower limit to the change of slope of the error probability curve. Using the technique described in [15], an upper bound of 8 to the minimum distance has been evaluated. As already mentioned, a lower bound of 5 is due to the construction method.

It must be observed that the onset of the error floor slope can not be predicted, since the multiplicity of low-weight codewords can not be assessed by simulation for code of this length.

G. Encoder and Decoder Implementation Complexity

The hardware implementation of a QC-LDPC code encoder is greatly simplified due to the quasi-cyclic structure of the parity check matrix. In fact, in this case the encoder can be implemented as the concatenation of shift registers [12].

The decoder implementation of a QC-LDPC code is simplified in two ways: the first point is that the memory needed to store the parity-check matrix description is greatly reduced due to the circulants-based structure. For the rate 15/16, code the decoder has to store the position of the 64 non-zero entries in the first row, since all remaining rows can be obtained by cyclic shifts of the 16 511x511 sub-matrices which form the parity matrix. For the remaining rates there is no need to store additional information, due to the method followed for the shortened parity matrix construction. The second complexity reduction is due to the regularity of the code, which makes the structure of the elementary arithmetic node performing the extrinsic information computation for both variable and check nodes fully regular, repeatable and reusable in a mixed parallel-serial decoder structure.

In addition, no significant changes to the decoder architecture are required for the shortened, lower rate codes, owing to the fact that the parity matrix of the shortened codes is simply obtained by removing the unneeded leftmost circulants.

A comparison of the estimated HW complexity with respect to published solutions for LDPC codes with high code rate is summarized in Table II.

<table>
<thead>
<tr>
<th>Code</th>
<th>Max Block Length [bits]</th>
<th>Total Memory [Kb]</th>
<th>Gate Count</th>
<th>Coded Data Rate [Mbit/s]</th>
<th>Notes</th>
</tr>
</thead>
</table>
| proposed      | 8176                    | 83                | 2 M        | 550                      | 15 it.
| WWiSE         | 1944                    | 100               | 468 K      | 565                      | 6 it. |
| AA-LDPC       | 2048                    | 52                | 220 K      | 640                      | 10 it.|

REFERENCES: WWiSE [17], AA-LDPC [18]

H. Adaptive Modulation Considerations

The code rate flexibility can be combined with M-QAM constellation choice to design an adaptive modulation system offering a good range of spectral efficiencies. In the target prototype system the modem can use all M-QAM constellations from 4 QAM up to 512 QAM, resulting in the spectral efficiencies reported in Table III.
ADAPTIVE CODED MODULATION SPECTRAL EFFICIENCIES

<table>
<thead>
<tr>
<th>Code Rate</th>
<th>4 QAM</th>
<th>16 QAM</th>
<th>64 QAM</th>
<th>128 QAM</th>
<th>256 QAM</th>
<th>512 QAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>15/16</td>
<td>1.87</td>
<td>3.75</td>
<td>5.63</td>
<td>6.56</td>
<td>7.50</td>
<td>8.44</td>
</tr>
<tr>
<td>13/14</td>
<td>1.86</td>
<td>3.71</td>
<td>5.57</td>
<td>6.50</td>
<td>7.43</td>
<td>8.36</td>
</tr>
<tr>
<td>11/12</td>
<td>1.83</td>
<td>3.67</td>
<td>5.50</td>
<td>6.42</td>
<td>7.33</td>
<td>8.25</td>
</tr>
<tr>
<td>9/10</td>
<td>1.80</td>
<td>3.60</td>
<td>5.40</td>
<td>6.30</td>
<td>7.20</td>
<td>8.10</td>
</tr>
</tbody>
</table>

IV. CARRIER RECOVERY

A. Synchronization Considerations

The front-end receiver has to operate efficiently at low SNR levels and with high order M-QAM constellations, in presence of significant levels of phase noise due to low-cost oscillators. Clock recovery and coarse carrier frequency recovery are not so critical and can be achieved by using standard methods, e.g. with Gardner algorithm and standard non-data aided methods, while carrier phase recovery poses several challenges.

Considering a standard Costas loop based carrier phase recovery, the following observations can be made:
- when the phase noise level increases, the loop bandwidth has to be increased to ensure good tracking
- with an increased bandwidth the contribution of thermal noise becomes more significant, and in turns this can lead to increased cycle slip rate

B. Phase Noise Effects

The effect of phase noise when the receiver employs a standard Costas Loop type carrier recovery can be seen in Fig.3. The corresponding BER curve shows a degradation which is the sum of two factors: the shift of the AWGN curve due to the thermal noise integrated in the carrier recovery bandwidth and the slope degradation caused by the non-gaussian error statistics.

The example shown exhibits the typical behaviour, where the BER curve is dominated by the slope caused by cycle slips and long error bursts.

C. Proposed Solution

As already mentioned, the design of carrier recovery for high-order modulations working at SNRs close to capacity is a challenging task. A fully blind solution does not lead to good results. Therefore the solution currently under study employs a pilot-aided algorithm.

The pilot aided scheme can be described as follows: assuming that the channel stream is divided into slots of \( N_p \) modulation symbol, into each slot there are \( N_p \) pilots while the remaining \( N_d - N_p \) symbols are data symbols.

The \( N_p \) pilots are used to derive a data aided ML estimate of the phase. The phase estimates thus obtained are passed to a smoothing filter. The filter coefficients are designed using the optimal MMSE method taking into account the overall noise spectral density. The filtered phase estimates are then fed to an interpolation filter, which produces an interpolated estimate between two consecutive pilot slots. Note that this introduces a delay of \( N_d \) symbols in the signal path.

The interpolated pilot estimates are then combined with the non-data aided estimates produced by the standard Costas loop type detector acting on the \( N_d - N_p \) remaining symbols.

In the described solution there are a number of parameters which have to be optimized for our adaptive radio link system conditions, which are discussed hereunder.

The first parameter to determine is the exact distribution of pilot symbols, which has to be optimized in terms of performance improvement and total overhead trade-off. From radio link traffic and air capacity considerations we have chosen to allocate to pilot symbols an overhead of 5% of the total air rate. The distribution of pilot symbols is currently under analysis, some preliminary results will be discussed in section V.

The smoothing filter acting on pilot estimates is designed to match the distribution of possible phase noise and thermal noise level for a selected radio link channel. However the sensitivity of the phase estimator performance to the overall noise spectral density shape remains to be investigated.

Finally, the interpolation filter uses at the moment a simple linear interpolation algorithm, however we believe that further improvements can be achieved by optimizing the interpolation function.

To summarize, the parts of the solution which are the subject of further work are:
- the smoothing filter acting on pilot phase estimates
- the interpolation filter generating intermediate phase estimates

V. SIMULATED PERFORMANCE

A. AWGN

Since the target application requires high-order \( M \)-QAM constellations to maximize spectral efficiency, we have simulated AWGN performance taking as reference a 128-QAM modulation. The simulation uses standard belief-propagation decoding with 20 iterations.

The BER results for the mother code and shortened codes down to a code rate of 9/10 are shown in Figure 1.
The 15/16 base code outperforms the RS(255,239,\(t=8\)) by more than 2 dB at a BER level of \(10^{-6}\). FER is less than 1 dB far from the pragmatic capacity [16] of 128-QAM at the same block length, as reported in Figure 2.

It can be seen that there is no significant change in the coding gain slope at high SNR levels for the base code and shortened codes down to 11/12. The 9/10 code shows a degradation in the coding gain slope around a value of \(E_b/N_0\) of 13.7 dB. To counteract the coding gain slope degradation for the shorter 9/10 code, we have measured the performance of a modified scheme where a BCH code with correction capability \(t=10\) and block length matching the information word length of the LDPC code. The results in Figure 2 show that the error floor effect of FER curves is reduced.

### B. Phase Noise

The phase noise simulation model synthesizes the phase noise spectral shape of a practical local oscillator used in the application at hand. Simulation results in terms of BER are shown in Figure 3, for the case of rate 15/16, 64-QAM modulation and the channelization most critical for the phase noise. They show preliminary results based on different pilot distribution and simple filtering of the resulting phase estimate. This point is the subject for further study.

In particular, the three curves refer to:
- the ideal AWGN channel for reference
- the basic scheme that uses an interleaver of length equal to 6 code words, and no filtering of the phase estimates
- the algorithm currently under analysis, which uses a simple filtering of phase estimates.

All curves have the same pilot overhead which is about 5% of the total air rate rate. From these curves it can be seen that the best algorithm found so far shows a loss of 0.8 dB at BER=10^{-7} with respect to the ideal AWGN case. Without filtering the inclusion of a long interleaver (6 code words, which exceeds the latency constraint) results in a further loss of 0.3 dB.

### C. Error floor of 9/10 code

In order to gain some insights on the error floor behavior of the 9/10 code, we have looked during long simulations for error patterns with low Hamming weight and low syndrome weight (near-codewords), which have been shown to contribute to the error floor [15]. Simulations have been run with 20 decoding iterations, and statistics for 1 million code
words or 30 blocks in error have been collected. All configurations with syndrome weight less than or equal to 8 and Hamming weight less than or equal to 6 have been collected. Their contribution to the frame error rate is shown in Table IV. Further investigations on this topic will be carried out in the FPGA prototype.

### Table IV

<table>
<thead>
<tr>
<th>Eb/No [dB]</th>
<th>FER</th>
<th>Near codeword found</th>
<th>Near codeword FER</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.5</td>
<td>1.2 x 10^{-4}</td>
<td>4</td>
<td>2.1 x 10^{-4}</td>
</tr>
<tr>
<td>14.0</td>
<td>1.1 x 10^{-4}</td>
<td>11</td>
<td>1 x 10^{-4}</td>
</tr>
</tbody>
</table>

### VI. Conclusions

In this paper we have presented some design issues related to adaptive LDPC coding and modulation techniques suitable for high-speed microwave radio transmission systems.

The flexible LDPC code performs within 1 dB of the pragmatic AWGN channel capacity, and outperforms conventional RS-based solutions by 2 dB in AWGN channel at a BER level of 10^{-6}. Preliminary results on the carrier synchronization algorithm, which has to work at the low SNR conditions imposed by the code and the relatively poor local oscillator behavior, have also been shown. The synchronization algorithm under analysis, under worst case conditions, performs within 0.8 dB from the AWGN channel case.

### Acknowledgment

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