LC Voltage Controlled Oscillators Design using MHS SCMOS3 0.5µm process

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Abstract—This paper deals with the design of an LC Voltage Controlled Oscillators using MHS SCMOS3 0.5 µm process. A sizing method is proposed to meet the WiFi and Bluetooth standards requirement. The layout of the circuit with CADENCE environment has been accomplished. Based on this layout, post layout simulations were performed and circuit improvement has been proposed in order to overcome parasites drawback.

I. INTRODUCTION

One of the largest growth areas in Radio-Frequency over the past decade has been in the application of mobile communication system, and it’s ever growing demand has caused renewed interest and generated more attention towards wireless architectures and applications.

Integrated voltage-controlled oscillators (VCOs) are essential building elements in the implementation of a single-chip radio in today’s communication systems. In recent years, the study and design of several types of VCOs have been proposed. Their main goal is the minimization of phase noise and the total integration including passive elements. In this context, this paper focuses on the implementation of a VCO for mobile radio application.

Section II covers circuit design details of the VCO core and presents experimental results. Section III describes the layout of the circuit and the result of post layout simulation. Section IV draws some conclusions.

II. LC VCO APPROACH DESIGN

A. LC VCO structure

The selected topology shown in Fig. 1 is a cross coupled CMOS oscillator based on a differential structure using both NMOS and PMOS cross coupled pairs [1]. The CMOS pairs provide negative resistance which offset losses of the LC resonator in order to compensate the tank loss. This oscillator is mainly composed of a tank resonator formed by inductor L and varactors M1A and M1B. The oscillation frequency range is controlled through two MOS accumulation varactors.

This structure is preferred to other structures for different reasons. For example, in comparison with the NMOS cross-coupled oscillator, studies show that the CMOS cross-coupled structure provides better noise performance. In fact, the CMOS cross-coupled LC-VCO offers better rise- and fall-time symmetry, which results in a smaller 1/f noise corner. From a consumption point of view, the VCO bias current must be doubled for the NMOS structure to obtain the same tank amplitude as in CMOS structure.

B. Equation formulation

According to Hajimiri [1], the equivalent model of the LC oscillator is shown in Fig. 2.

\[ C_{\text{load}} = C_{\text{PMOS}} + C_{\text{NMOS}} \]

\[ g_{\text{m, NMOS}} = g_{\text{m, PMOS}} \]

\[ C_{\text{NMOS}} = C_{\text{gs, NMOS}} + C_{\text{db, NMOS}} + 4C_{\text{gd, NMOS}} \]  

\[ C_{\text{PMOS}} = C_{\text{gs, PMOS}} + C_{\text{db, PMOS}} + 4C_{\text{gd, PMOS}} \]  

\[ g_{\text{m, NMOS}}, \quad g_{\text{m, PMOS}} \] are respectively the small signal transconductances of the NMOS and PMOS transistors.
\( g_{on}, g_{op} \) are respectively the output conductances of the NMOS and PMOS transistors.

\( R_s, R_p, C_s, C_p \) and \( L \) form the equivalent symmetric model elements of spiral inductor with parasitic elements [2] as shown in Fig. 3.

\( R_s, \) \( C_s, \) are respectively the series capacitance and resistance.

\( R_p, C_p \) are respectively the shunt resistance and capacitance and are calculated using the following expressions:

\[
R_p = \frac{1}{C_p} \left( 1 + \frac{R_s}{(2\pi f_0)^2} \right) \left( \frac{R_s}{C_p} \right)^2
\]

(3)

\[
C_p = \frac{C_s}{1 + \left( \frac{R_s}{(2\pi f_0)^2} \right) \left( \frac{R_s}{C_p} \right)^2}
\]

(4)

\( R_{sl1} \) and \( C_{sl1} \) are respectively the series resistance and capacitance extracted using ASITIC software [3].

The effective parallel conductance of the inductor is given by the equation (5):

\[
g_L = \frac{1}{R_p} + \frac{R_s}{(L2\pi f_0)^2}
\]

(5)

Varactor is made with PMOS transistors in accumulation mode. Its model is composed of a resistor \( R_v \) in series with a capacitor \( C_v \).

The effective parallel conductance of the varactor is given by equation (6):

\[
g_v = (C_{v_{max}}2\pi f_0)^2 R_v
\]

(6)

Hence, the conductance of the resonator \( g_{tank} \) is defined by the equation (7)

\[
g_{tank} = \frac{1}{2} \left( \lambda_n + \lambda_p \right) \left( \frac{L_{tank}}{2} \right) + g_s + g_f
\]

(7)

\( \lambda_n \) and \( \lambda_p \) are respectively the channel length modulation of NMOS and PMOS transistors forming the active part. The total capacitance \( C_{tot,max} \) and inductance \( L_{tot} \) of the oscillator are defined respectively by the expressions (8) and (9).

\[
C_{tot,max} = \frac{1}{2} \left( C_{PMOS} + C_{NMOS} + C_P + C_{v_{max}} + C_{load} \right)
\]

(8)

\[
L_{tot} = 2L
\]

(9)

C. LC VCO sizing

The flow chart given in Fig. 4 presents the design approach used to size the LC VCO.

We start by defining the specifications of the VCO by choosing a range of variation around 2.4 GHz (WiFi (b/g), Bluetooth), limiting a power consumption to 12 mW, a bias current 4mA and a minimum tank amplitude of 1V.

After determining inductance and varactor’s parameters, the value of the conductance of the resonator \( g_{tank} \) defined by the equation (7) has been deduced.

The next step for this phase of design was to ensure the startup condition [1].

\[
|g_{neg}| \geq \alpha_{min} g_{tank}
\]

(10)

Where \( \alpha_{min} \) is the conservative minimum small signal loop gain fixed at 2 and \( g_{neg} \) is the effective negative conductance defined by the expression (11).

\[
g_{neg} = \frac{1}{R_{neg}} = \frac{g_{m,n} + g_{m,p}}{2}
\]

(11)

To eliminate the 1/f phase noise; it is essential to have a symmetrical structure with \( g_{m,n} = g_{m,p} = g_m \) [1]. Hence, the width of active transistors has been deduced.
Finally, the essential characteristics as the tank amplitude, minimum frequency, maximum frequency and phase noise were found.

The tank amplitude is defined by the expression (12) which should be greater than a minimum magnitude required, $V_{\text{tank,min}}$, in order to provide a high voltage swing, for the stage connected at the output of the VCO.

$$V_{\text{tan}} = \frac{4 I_{\text{bias}}}{\pi g_{\text{tan}}}$$

(12)

Based on the expression (8) and (9), the minimum frequency is given by equation (13).

$$f_{\text{min}} = \frac{1}{2\pi \sqrt{L_{\text{tot}}C_{\text{tot,max}}}}$$

(13)

According to the model of Hajimiri [4], phase noise in the LC oscillator is given by the expression (14).

$$PN = 10\log_{10}\left(\frac{1}{8\pi f_{\text{min}}^2 V_{\text{sat}}} \left(\frac{2\pi}{\gamma \pi} \right)^{1/2} \left(\frac{K T R}{3} + 2K T R + 2K T R \left(g_{\text{d0n}} + g_{\text{d0p}}\right)\right)\right)$$

(14)

Where $g_{\text{d0n}}$ and $g_{\text{d0p}}$ are the channel conductances for NMOS and PMOS transistors respectively, defined by the expression (15).

$$g_{\text{d0n}} = \frac{I_{\text{bias}}}{l_{\text{canal}} E_{\text{sat,n}}} \quad g_{\text{d0p}} = \frac{I_{\text{bias}}}{l_{\text{canal}} E_{\text{sat,p}}}$$

(15)

$E_{\text{sat,n}}$ and $E_{\text{sat,p}}$ are respectively the saturation electric field of NMOS et PMOS transistors.

$L_{\text{canal}}$ is the minimum channel length allowed by the used process.

A. Simulation results

The LC VCO described above is simulated using RF-SPECTRE simulator under CADENCE environment using MHS SCMOS 0.5µm technology.

The output of the LC VCO is depicted in Fig. 5, the amplitude of oscillations is 1.13V which is sufficiently large at the mixer entrance.

The oscillation frequency varies between 2.2 GHz and 2.5 GHz giving a range of 335 MHz. In this feature, the sensitivity of the frequency compared to the control voltage is equal to 251 MHz/V.

As shown in Fig. 6, phase noise is plotted versus offset frequency from 2.4 GHz (carrier). The phase-noise measurement is -100.3 dBc/Hz at 100 KHz, -117 dBc/Hz at 600 KHz and -121.5 dBc/Hz at 1 MHz.

III. IMPLEMENTATION

A. Layout description

With Virtuoso Layout Edition of CADENCE environment, the layout of CMOS cross coupled oscillator shown in Fig. 7 has been realized. Due to the differential nature of the circuit, a special attention was paid to the symmetry of the design.

In the layout of the varactor, we noted the presence of eight fingers to reduce the resistance of the gate. All drains and sources of the varactor transistors are connected to operate in accumulation mode.

The inductors used in the circuit are generated using ASITIC tool. Then they were drawn under CADENCE while respecting their geometric dimensions.

To reduce the effect of thermal or process linear gradients that may be present in an integrated circuit, the common centroid technique were used for the implementation of the current mirror and the two differential pairs.

The plots of entry and exit are added to ensure the circuit test. The surface of the chip is 0.026 mm². The total area of the layout is 0.426 mm².
B. Post layout simulations

First, a Post Layout simulation without parasitic elements was performed. It is important to mention that the performances are comparable to those of schematic with a slight shift of the oscillation frequency tuning range. Furthermore, a Post Layout simulation with RC parasitic elements was realized, an important shift is obtained as is summarized in Table 1.

Fig. 8 shows that during the Post-Layout simulation with RC parasitic elements, the swing of the capacitor versus control voltage remains almost constant with a shift upward. This shift event is due to the addition of parasitic capacitances.

The differential output signals represented in Fig. 9 shows that the amplitude of oscillations is reduced to 560 mV. This is mainly due to the presence of the parasitic resistances. An oscillation frequency degradation is also observed. In fact, the frequency varies between 2 GHz and 2.2 GHz. The range of frequency is then 200 MHz.

By comparing the two simulations post layout with parasitic elements and pre layout, the oscillation frequency degradation is about 11%.

This difference is mainly explained by the effect of parasitic capacitances and resistances added by the layout. Therefore, these results have to be improved to cover the desired frequency range (around 2.4 GHz).

C. Performance Improvement

The results of the post layout simulation with RC parasitic elements show a degradation of oscillator characteristics. In order to cover the desired frequency range (around 2.4 GHz), the idea consists on tuning the oscillation frequency model used in the sizing step. This correction is performed by variations of some circuit parameters, taking into account the impact of layout. In order to perform this correction, an experience plane is established showing the parameters variation way to improve circuit performances.

According to this correction, the obtained shifted central frequency is equal to 2.65 GHz. So that, in post layout simulation with RC parasitic elements, the obtained frequency will respect the expected value.

Table 2 shows a comparison between the initial values of calculated parameters and the new values obtained after the improvement. We can observe the reduction of the transistors size of the varactor and the two differential pairs affecting the frequency range.

The pre layout simulation done with the new parameters shows that the range of frequency variation is between 2.5 and 2.8 GHz.

The results (see Table 3) in post layout simulation with RC parasitic elements, show that the expected frequency range was really met and respect the specifications (around the 2.4 GHz).
### Table 2
**IMPROVED PARAMETERS VALUE**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Initial values</th>
<th>Improved values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wn(µm)</td>
<td>68</td>
<td>48</td>
</tr>
<tr>
<td>Wd(µm)</td>
<td>206</td>
<td>144</td>
</tr>
<tr>
<td>Wv(µm)</td>
<td>780</td>
<td>640</td>
</tr>
<tr>
<td>L(nH)</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Isat(mA)</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Ng</td>
<td>80</td>
<td>80</td>
</tr>
</tbody>
</table>

### Table 3
**IMPROVED POST-LAYOUT RESULTS**

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>Circuit performances</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fmin (GHz)</td>
<td>2.348</td>
</tr>
<tr>
<td>Fmax (GHz)</td>
<td>2.452</td>
</tr>
<tr>
<td>Phase noise at 1MHz (dBc/Hz)</td>
<td>-116</td>
</tr>
<tr>
<td>Vtank(mV)</td>
<td>501</td>
</tr>
<tr>
<td>Kvco(MHz/V)</td>
<td>142</td>
</tr>
</tbody>
</table>

### IV. CONCLUSION

A 2.4GHz CMOS VCO implementation using MHS SCMOS3 0.5µm process is presented. The results in pre layout simulation were excellent and meet the application requirements.

In post layout simulation with RC parasitic elements, a degradation of oscillator characteristics is found. As a solution, a correction is performed by variations of some circuit parameters, taking into account the impact of layout. VCO post layout simulations show that good performances are reached for the frequency range [2.348 GHz, 2.452 GHz], by reducing the transistors size of both the varactor and the active part.

### REFERENCES


